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THOMAS J D AMICO
DICKSTEIN SHAPIRO MORIN AND OSHINSKY
2101 L STREET N W
WASHINGTON, DC 200371526

EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/123,430	Applicant(s) YATES, DONALD L.	
	Examiner Brook Kebede	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,7,9-13,15,17,18,20-23,25-27,44,52,58 and 61-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,23,52,58,65 and 72* is/are allowed.

6)☒ Claim(s) *1,6,7,9,10,12,15,17,18,20-22,25-27,44,61,62,64,66-71 and 73-77* is/are rejected.

7)☒ Claim(s) *13 and 63* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed under 37 C.F.R. 1.116, after the final Office action of March 25, 2004 is entered and placed in the record.

2. The Examiner withdraws the indicated allowability of claims 17, 18, 21, 68, 71, 74, 75, 76, and 77 and the finality of the Office action that was mailed on January 30, 2004 because the amendment filed on March 25, 2004 under 37 C.F.R. 1.116 place the application in better form by clarifying issues that raised under 35 U.S.C. 112 second Paragraph in the Office action of January 30, 2004. Since applicant's amendment/response did not place the application in condition for allowance, the new final Office action is set forth herein below. As of record, this final Office action is necessitated by the amendments filed on October 31, 2003 and January 30, 2004 respectively.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 68-71 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 68 recites the limitation "reducing said processing bath volume of said semiconductor processing bath in a processing vessel by rapidly removing an upper portion of a semiconductor processing fluid presented said processing fluid" in lines 5-6. However, the recited claim lacks clarity in its meaning and scope because it is not clear how the volume the

bath can be reduced by rapidly removing an upper portion of a semiconductor processing fluid presented said I processing fluid. Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 69-71 are also rejected as being dependent of the rejected independent base claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 44 is rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al., (USPAT/5,275,184).

Re claim 44, Nishizawa et al. disclose a method for reducing the contaminants on a silicon wafer during a wet etching process, said method comprising: immersing a wafer boat suspended on a lifting arm in an etching vessel having an aqueous hydrofluoric acid solution therein for a sufficient time to etch said silicon wafer; and rapidly removing said wafer boat from said etching vessel to remove surface contaminants residing; on the upper surface of said aqueous hydrofluoric acid solution by an upward movement of said arm, thereby causing an upper portion of said aqueous hydrofluoric acid solution to spill out of said vessel to reduce the

amount of said aqueous hydrofluoric acid solution in said etching vessel(see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14; Col. 11, lines 18-20).

7. Claims 66 and 73 are rejected under 35 U.S.C. 102(e) as being anticipated by Kamikawa et al. (US/6,131,588).

Re claim 66, Kamikawa disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: immersing the semiconductor wafers in a semiconductor etching bath ; and rapidly removing an upper portion of a semiconductor processing fluid present in said etching bath by rapidly removing a wafer boat containing said wafers from said bath to permit flow of said upper portion of said processing fluid and thereby break eddy currents holding said surface contaminants at said air/liquid interface (see Figs. 1-30)

Re claim 73, Kamikawa disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: processing the semiconductor wafers in a semiconductor etching solution; and rapidly removing an upper portion of the semiconductor etching solution by rapidly removing a wafer boat containing said wafers from said bath to permit flow of said upper portion of said processing fluid and thereby break surface tension forces holding said surface contaminants at said air/liquid interface (see Figs. 1-30).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1, 6, 7, 9, 12, 15, 17, 18, 20-22, 25, 26, 61, 64, 67, 68, 71, and 74-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (USPAT/5,275,184) in view of Hayami et al. (USPAT/5,474,616).

Re claim 1, Nishizawa et al. disclose a method for removing surface contaminants from air/liquid interface of a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising: immersing wafers in a bath of semiconductor processing fluid (see Fig. 2); processing said wafers immersed in said bath of semiconductor processing fluid contained within said processing apparatus; and reducing the volume of semiconductor processing fluid contained in the processing apparatus by rapidly displacing an upper portion semiconductor processing fluid present in the bath while the wafers remain immersed in a lower portion of the bath of semiconductor processing fluid in the processing apparatus to remove the surface contaminants from the air/liquid interface (see Fig. 2 and Col. 2, lines 62-67 through Col. 5, lines 1-27 and see abstract).

However, Nishizawa et al. do not specifically disclose reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the

wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 6, as applied to claim 1 above, both Nishizawa et al. and Hayami et al. disclose all the claimed limitations including the limitation wherein the contaminants include silica (see Nishizawa et al Fig. 2 and Hayami et al. Figs. 41 and 42).

Re claim 7, Nishizawa et al. do not specifically disclose a method for reducing the contamination on a semiconductor wafer from wet etching bath comprising: immersing the semiconductor wafer in the wet etching bath; processing the semiconductor wafer in the wet etching bath by continuously feeding an etching fluid; and remove surface contaminants form an air/liquid interface of the wet etching bath while retaining the semiconductor wafer in a lower portion of the etching fluid contained within the processing apparatus; and subsequently removing of the wafer from the bath (see Fig. 2 and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

However, Nishizawa et al. disclose subsequently rapidly reducing a volume of the etching bath contained within a processing apparatus by removing a substantial portion of an upper portion of the etching fluid from the processing apparatus to reduce the overall volume of etching fluid in the processing apparatus.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the subsequent removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 9, as applied to claim 7 above, both Nishizawa et al. and Hayami et al. disclose all the claimed limitations including the limitation wherein the upper portion of the etching fluid is removed by draining a top portion of the etching fluid from wet etching bath (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 12, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing cleaning bath for processing semiconductor wafers the method comprising: immersing the wafers in the semiconductor wafers ins the semiconductor processing cleaning bath; and reducing a volume of fluid in the semiconductor processing cleaning bath before removing the semiconductor wafers by rapidly removing form a processing apparatus an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the

bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the subsequent removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door

would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 15, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing cleaning bath for processing semiconductor wafers the method comprising: immersing the wafers in the semiconductor processing cleaning bath contained in process apparatus; rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are immersed in the bath from processing apparatus (see Fig. 2).

However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath to rapidly reduce a liquid holding capacity of the processing apparatus and to remove the surface contaminants form the air/liquid interface.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath to rapidly reduce a liquid holding capacity of the processing apparatus and to remove the surface contaminants form the air/liquid interface (see Fig. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with removing a

portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath to rapidly reduce a liquid holding capacity of the processing apparatus and to remove the surface contaminants form the air/liquid interface to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus as taught by Hayami et al. because the use of the telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 17, Nishizawa et al. disclose a method for etching a semiconductor wafer, said method comprising: placing an aqueous hydrofluoric acid etching fluid into a wet etching vessel; immersing said semiconductor wafer in said etching fluid; contacting said semiconductor wafer with said etching fluid for a predetermined time; reducing a volume of said etching fluid in which said wafers are immersed by rapidly removing a portion of said etching fluid from the upper surface of said etching fluid to reduce an overall volume of fluid contained in said wet etching vessel while keeping said semiconductor wafer immersed in a remaining portion of said etching fluid; and removing said semiconductor wafer from said etching fluid(see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14; Col. 11, lines 18-20).

However, Nishizawa et al. do not specifically disclose the remaining cleaning (etching) liquid portion having smaller volume than the process volume.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface so that the remaining of portion process fluid volume is smaller tan the initial portion process fluid volume (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the subsequent removal of a portion of the etching (cleaning) liquid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing liquid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface so that the final remaining cleaning liquid volume is

lower than that of the initial process volume of the cleaning liquid as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath as result the remaining liquid volume is lower than that of the initial process liquid volume.

Re claim 18 as applied to claim 17 above, both Nishizawa et al. and Hayami et al. disclose all the claimed limitations including the limitation wherein the semiconductor is a silicon wafer (see Nishizawa et al. abstract)

Re claim 20, as applied to claim 17 above, both Nishizawa et al. and Hayami et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from an upper surface of the wet etching vessel by draining of the top portion of the etching fluid from the wet etching vessel (see Nishizawa et al. Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 21, Nishizawa et al. disclose a method for removing surface contaminants from air/liquid interface of a semiconductor processing bath (i.e., an etching bath) for processing semiconductor wafers the method comprising: placing an etching fluid into a wet etching vessel; placing wafers in a bath of semiconductor processing fluid (see Fig. 2); contacting the semiconductor wafer with etching fluid for predetermined time; and reducing an overall volume capacity of semiconductor processing fluid contained in the processing apparatus by rapidly displacing an upper portion semiconductor processing fluid present in the bath while the wafers remain immersed in a lower portion of the bath of semiconductor processing fluid in the

processing apparatus to remove the surface contaminants from the air/liquid interface (see Fig. 2 and Col. 2, lines 62-67 through Col. 5, lines 1-27 and see abstract).

However, Nishizawa et al. do not specifically disclose reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus

while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 22, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for predetermined time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath and reducing a liquid capacity of the wet etch vessel while the semiconductor wafer remains immersed in a lower portion of the etching fluid.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing

fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 25, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid (i.e., an aqueous HF solution) into a wet etching vessel; immersing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; and reducing a fluid-containing volume of the wet etching vessel so as to rapidly displace a portion of the etching fluid from the upper surface

of wet etching vessel at a non-constant velocity while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath while the semiconductor wafer is remain in the bath immersed in the remaining portion of the etching solution (see Fig. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 26, as applied to claim 17 above, both Nishizawa et al. and Hayami et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from the upper surface of the wet etching vessel by physically removing a top portion of the etching fluid from the wet etching bath (see Fig. 2).

Re claims 61, 64, and 67 Nishizawa et al. disclose a method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath for processing semiconductor wafers, said method comprising: immersing said semiconductor wafers in the semiconductor processing bath contained in a process apparatus; reducing a volume of said semiconductor processing bath contained within a processing the apparatus by rapidly removing an upper portion of a semiconductor processing fluid present in said processing apparatus, while said semiconductor wafers are immersed in a remaining lower portion of said semiconductor processing bath, to permit flow of said upper portion of said processing bath out of said processing apparatus and thereby break eddy currents holding said surface contaminants at said air/liquid interface (see Fig. 2).

However, Nishizawa et al. do not specifically disclose reducing the total volume of liquid contained within the processing apparatus by removing the upper portion of the semiconductor processing bathe by telescopically collapsing/hingedly releasing door that located upper portion of the processing apparatus.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing/ telescopically collapsing door located at an upper portion of the bath that allows reducing of the total volume of the liquid contained by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released/ telescopically collapsing door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce the total volume of liquid contained within the processing apparatus by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

In light of the rejection 35 U.S.C. § 112 second Paragraph that set forth herein above in Paragraph 4, claims 68 and 71 are rejected based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

Re claim 68, 71 and 74, Nishizawa et al. disclose a method for removing surface contaminants from air/liquid interface of a semiconductor processing bath (i.e., an etching bath)

for processing semiconductor wafers the method comprising: immersing wafers in a bath of semiconductor processing fluid (see Fig. 2); processing said wafers immersed in said bath of semiconductor processing fluid contained within said processing apparatus; and reducing an overall volume capacity of semiconductor processing fluid contained in the processing apparatus by rapidly displacing an upper portion semiconductor processing fluid present in the bath while the wafers remain immersed in a lower portion of the bath of semiconductor processing fluid in the processing apparatus to remove the surface contaminants from the air/liquid interface (see Fig. 2 and Col. 2, lines 62-67 through Col. 5, lines 1-27 and see abstract).

However, Nishizawa et al. do not specifically disclose reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus by hingedly releasing /telescopically collapsing a door located at an upper portion of the bath while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing/telescopically collapsing a door located at an upper portion of the bath that allows reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing/telescopically collapsing a door located at an upper portion of the bath in order to reduce a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 75, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising: processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently reducing a volume of etching fluid in said wet etching bath and breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to reduce an overall volume of fluid contained within said processing vessel, said act of breaking said eddy currents further releasing surface contaminants which are formed at an

air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents; and subsequently removing said semiconductor wafer from said wet etching bath. (see Fig. 2).

However, Nishizawa et al. do not specifically disclose reducing overall (total) volume of liquid (fluid) contained within the processing apparatus by removing the upper portion of the semiconductor processing bathe by telescopically collapsing/hingedly releasing door located upper portion of the processing apparatus.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing/ telescopically collapsing door located at an upper portion of the bath that allows reducing of the total volume of the liquid contained by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface subsequently removing the semiconductor wafer from the wet etching processing bath having reduced overall volume of fluid (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released/ telescopically collapsing door so to allow the removal of a portion of the etching

(cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce the total volume of liquid contained within the processing apparatus by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 76, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising: processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently reducing a volume of said wet etching fluid and breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from processing, vessel containing said wet etching bath and reduce an overall volume of fluid contained within said processing v, said act of breaking said surface tension forces further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents; and subsequently removing said semiconductor wafer from said wet etching bath (see Fig. 2).

However, Nishizawa et al. do not specifically disclose reducing overall (total) volume of liquid (fluid) contained within the processing apparatus by removing the upper portion of the

semiconductor processing bathe by telescopically collapsing/hingedly releasing door located upper portion of the processing apparatus.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing/ telescopically collapsing door located at an upper portion of the bath that allows reducing of the total volume of the liquid contained by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface subsequently removing the semiconductor wafer from the wet etching processing bath having reduced overall volume of fluid (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released/ telescopically collapsing door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce the total volume of liquid contained within the processing apparatus by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the

bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

Re claim 77, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer, said method comprising: processing said semiconductor wafer in a static etching bath containing an etching fluid; and reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce volume of fluid contained within said container while said semiconductor wafer is in a remaining portion of said static etching bath (see Fig. 2).

However, Nishizawa et al. do not specifically disclose reducing overall (total) volume of liquid (fluid) contained within the processing apparatus by removing the upper portion of the semiconductor processing bath such that the container holds less fluid while the semiconductor wafer is immersed in a remaining portion of the static etching bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the static etching bath, by hingedly releasing/ telescopically collapsing door located at an upper portion of the bath that allows reducing of the total volume of the liquid contained by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface

subsequently removing the semiconductor wafer from the wet etching processing bath such that the container holds less fluid while the semiconductor wafer is immersed in a remaining portion of the static etching bath (see Hayami et al. Figs. 41 and 42).

Both Nishizawa et al. and Hayami et al. teachings directed to apparatus and a method of cleaning articles such as semiconductor wafers using a cleaning bath. Hence, the teachings of Nishizawa et al. and Hayami et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's claimed invention was made to provide Nishizawa et al. reference with a hingedly released/ telescopically collapsing door so to allow the removal of a portion of the etching (cleaning) fluid from upper surface of the etching bath liquid by hingedly releasing a door located at an upper portion of the bath in order to reduce the total volume of liquid contained within the processing apparatus by reducing a liquid holding capacity of the processing apparatus and thereby rapidly displacing an upper portion of the semiconductor processing fluid form the processing apparatus while the wafer remain fully immersed on a lower portion of the bath of the semiconductor processing fluid within the processing apparatus to remove the surface contaminants form the air/liquid interface as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching (cleaning) bath when the door opened and that lowers the over all volume of the process bath fluid containing capacity and displacing the cleaning fluid while the wafer remains in the cleaning bath.

10. Claims 10, 27, 62, 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (USPAT/5,275,184) and Hayami et al. (USPAT/5,474,616), as applied to claim 26 above in Paragraph 9, and further in view of Itoh et al., (USPAT/5,795,401).

Re claim 10, as applied in claim 9 in Paragraph 7 above, both Nishizawa et al. and Hayami et al. in combination teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to provide the combination teachings of Nishizawa et al. and Hayami et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 27, as applied in claim 26 in Paragraph 9 above, both Nishizawa et al. and Hayami et al. in combination teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to provide the combination teachings of Nishizawa et al. and Hayami et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 62, as applied to claim 61 in Paragraph 9 above, both Nishizawa et al. and Hayami et al. in combination teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to provide the combination teachings of Nishizawa et al. and Hayami et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

In light of the rejection 35 U.S.C. § 112 second Paragraph that set forth herein above in Paragraph 4, claim 69 is rejected based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

Re claim 69, as applied to claim 68 in Paragraph 9 above, both Nishizawa et al. and Hayami et al. in combination teach all the limitation in the claimed limitations except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to provide the combination teachings of Nishizawa et al. and Hayami et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Allowable Subject Matter

11. Claims 11, 23, 52, 58, 65, 72 are allowed over prior art of record.

12. Claims 13, 63 and 70 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claim 70 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Response to Arguments

14. Applicant's arguments with respect to claims 1, 6, 7, 9, 10, 12, 15, 17, 18, 20-22, 25-27, 44, 61, 62, 64, 66-71, and 73-77 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
April 10, 2004

George Fourson
Primary Examiner